

Model Name: GA-Z68MX-UD2H-B3 Revision 1.0

SHEET TITLE

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03	BLOCK DIAGRAM
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05	CPU_LGA1155-B
06	CPU_LGA1155-C
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08	DDR III CHANNEL B 1,2
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11	PCH_HOST,SATA,PCI
12	PCH_GPIO,CTRL,AUDIO
13	PCH_PWR,GND
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15	PCI EXPRESS*16 SWITCH
16	PCI EXPRESS*8 SLOT
17	PCI EXPRESS*1,*4,SWITCH
18	ITE 8728 LPC IO
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22	FP,FUSB,SPK,SATALED
23	ALC889
24	REAR AUDIO JACK
25	LAN RTL8111E
26	DISCRETE POWER
27	ATX,TPM

SHEET TITLE

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30	VCORE ISL6364_1,PWM
31	VCORE ISL6364_2,VCORE
32	VCORE ISL6364_3,VAXG
33	VCORE ISL6364_4,IT8275C
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35	F_USB3.0-EJ168
36	Marvell 9172 SATA3

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Cover Sheet			
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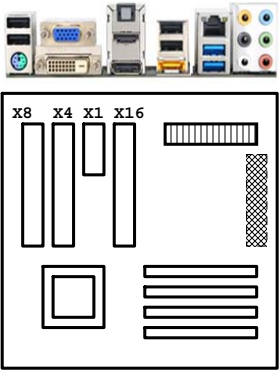
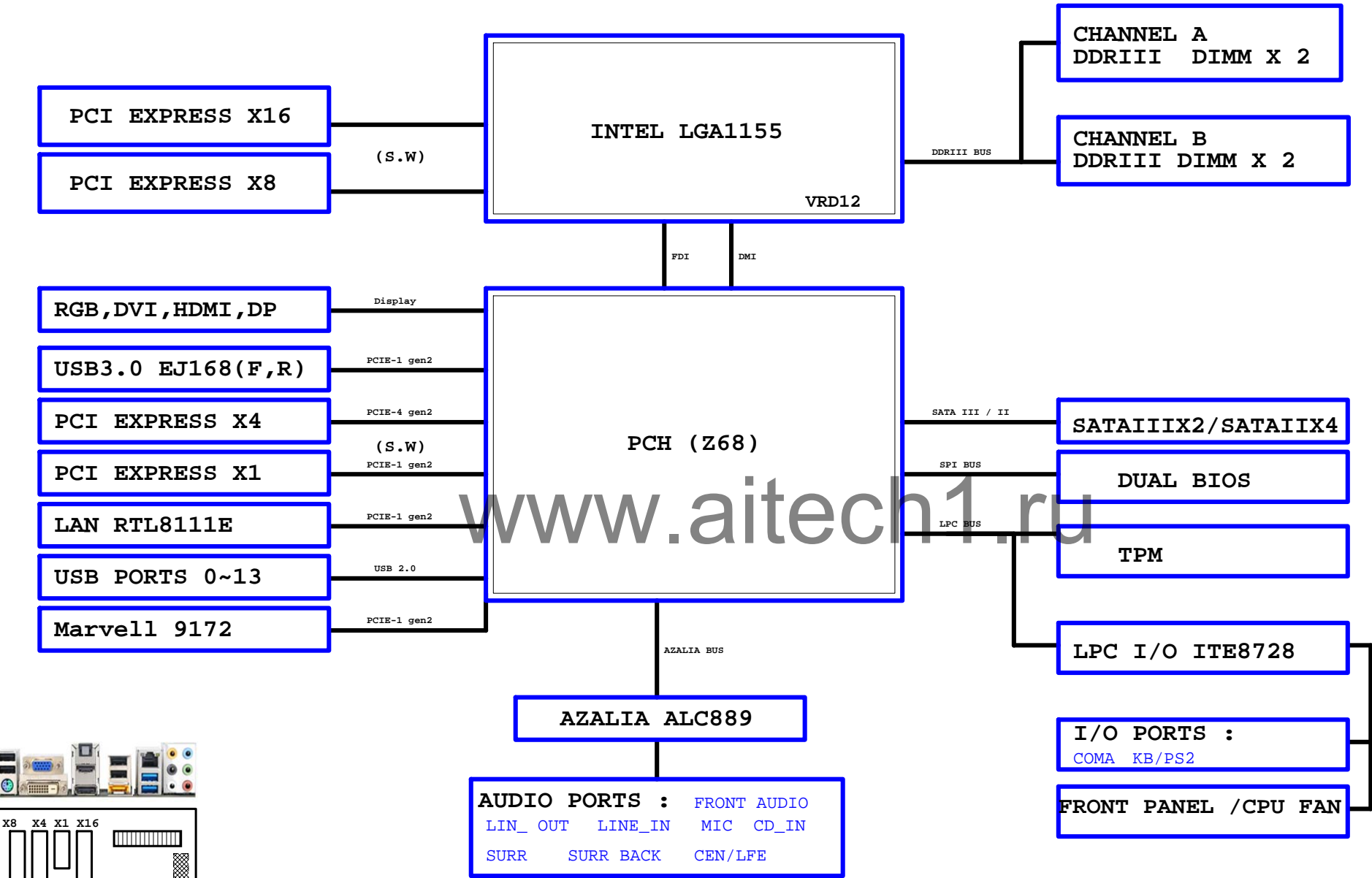
Circuit or PCB layout change

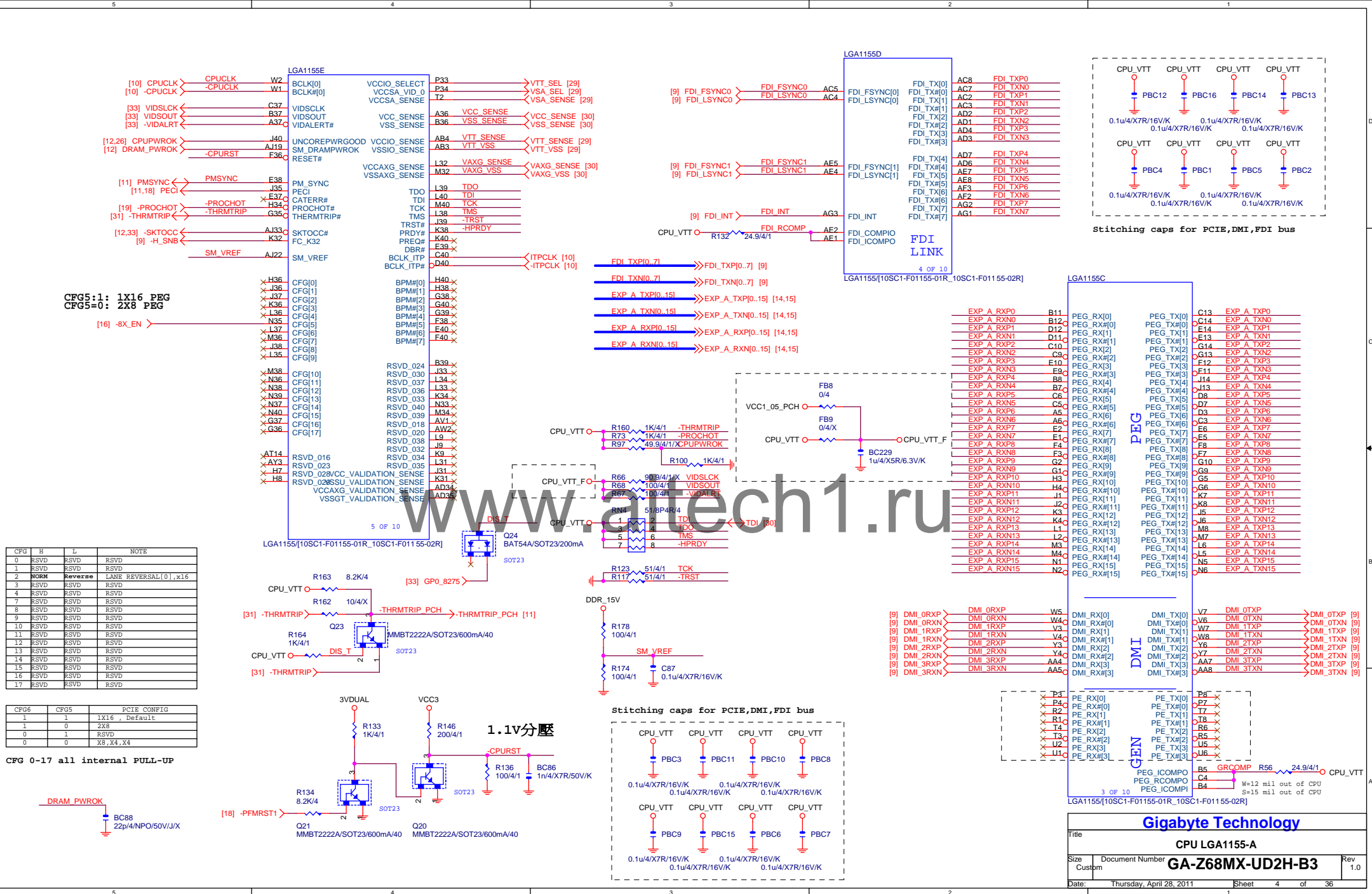
Component value change history

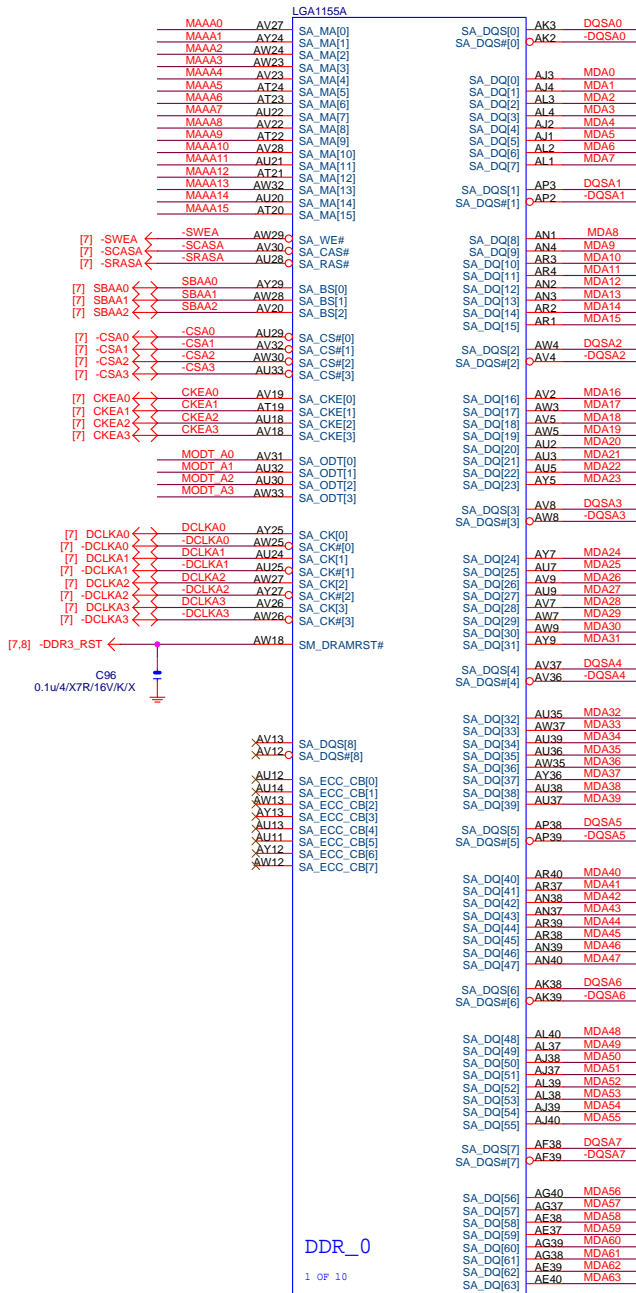
2011/04/28

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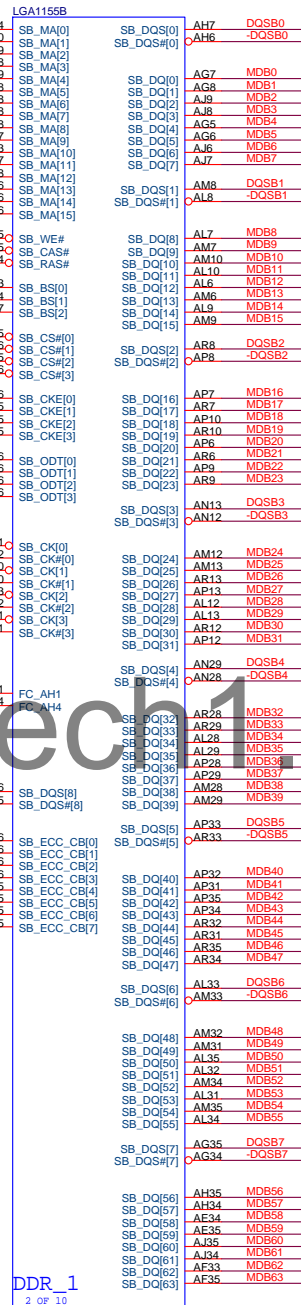
BLOCK DIAGRAM



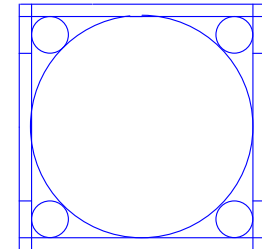




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CR
CPU RETENTION X

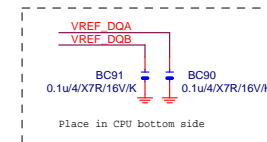


Need check the new CPU ME

LGA1155_P

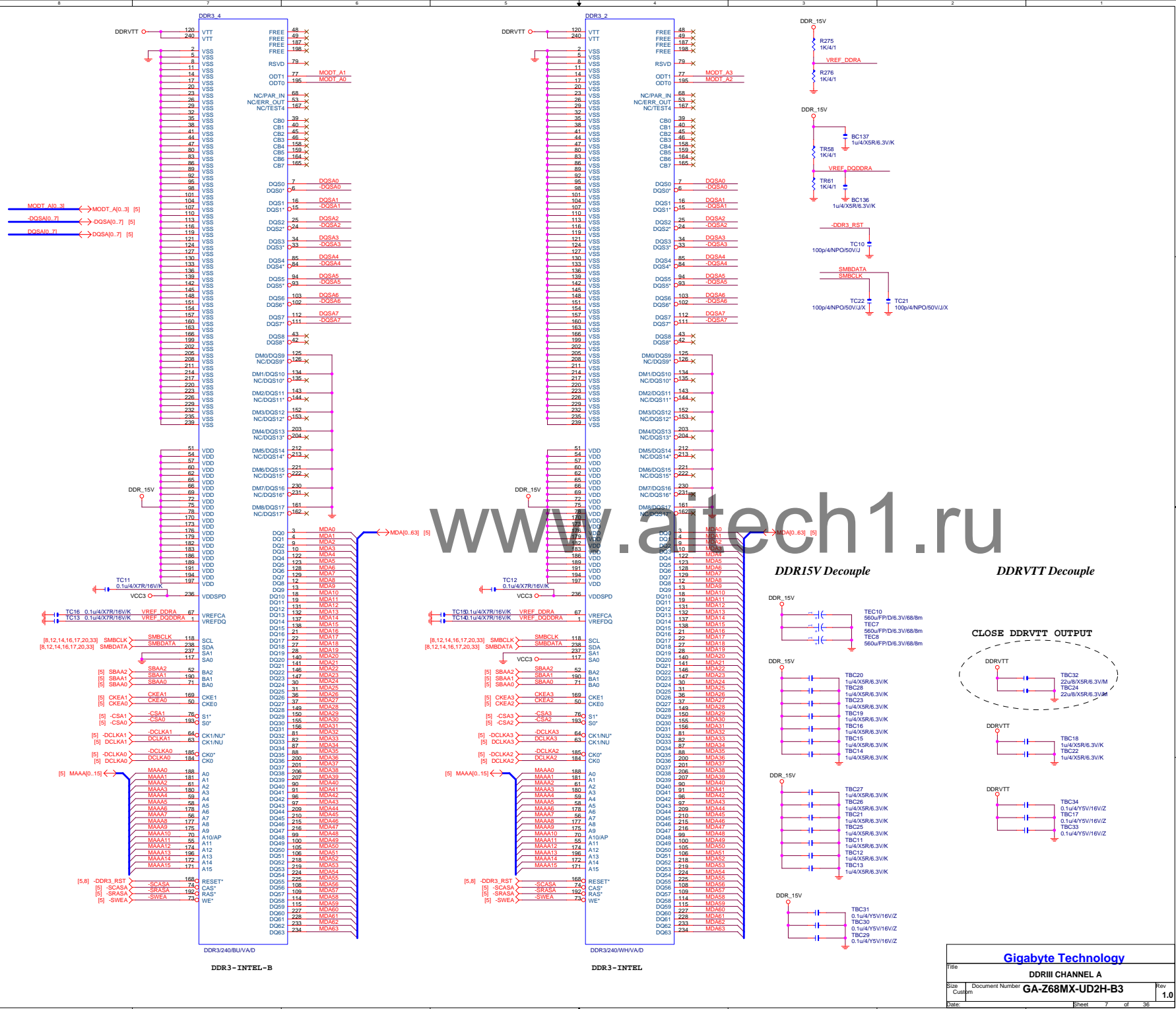


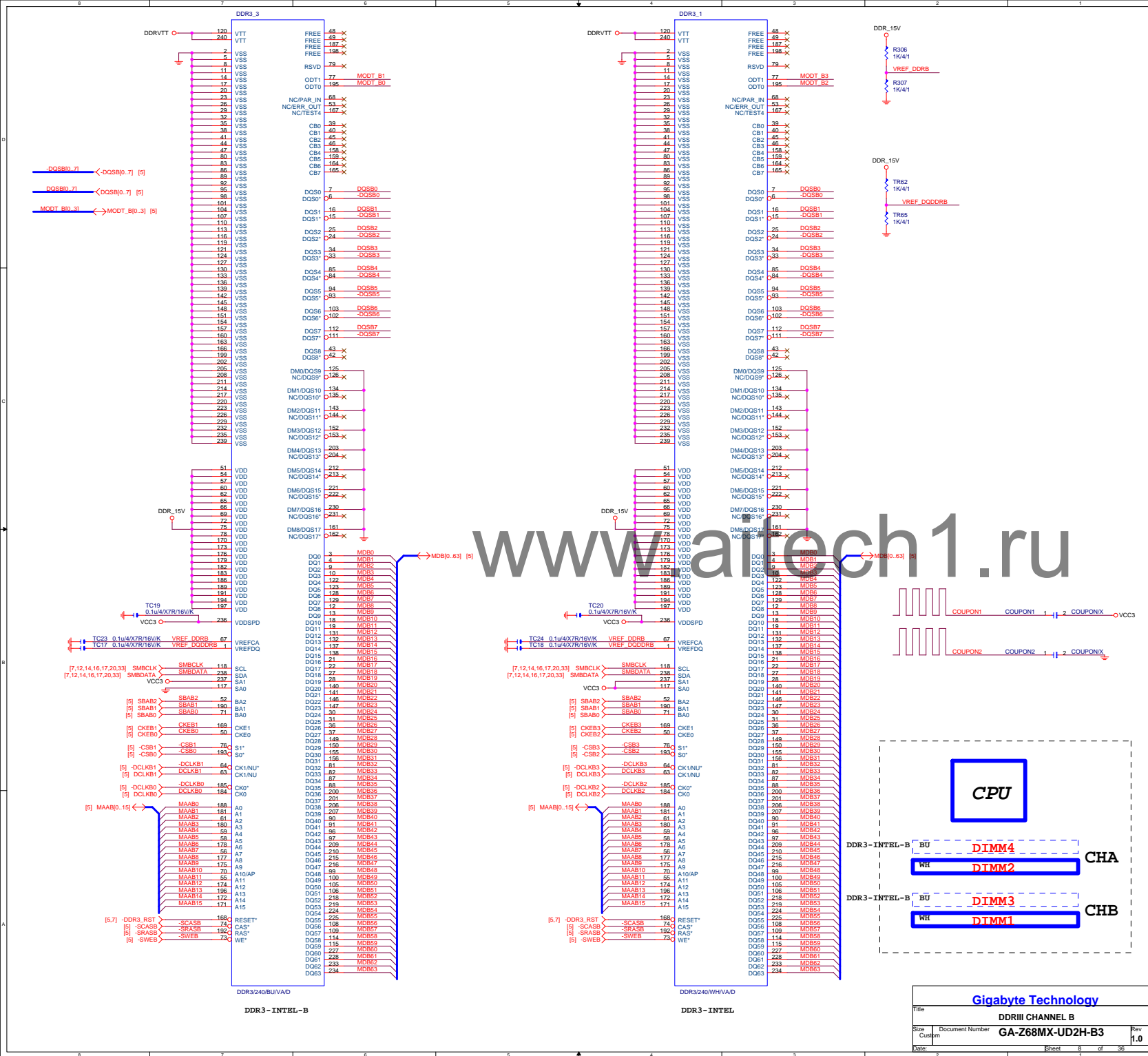
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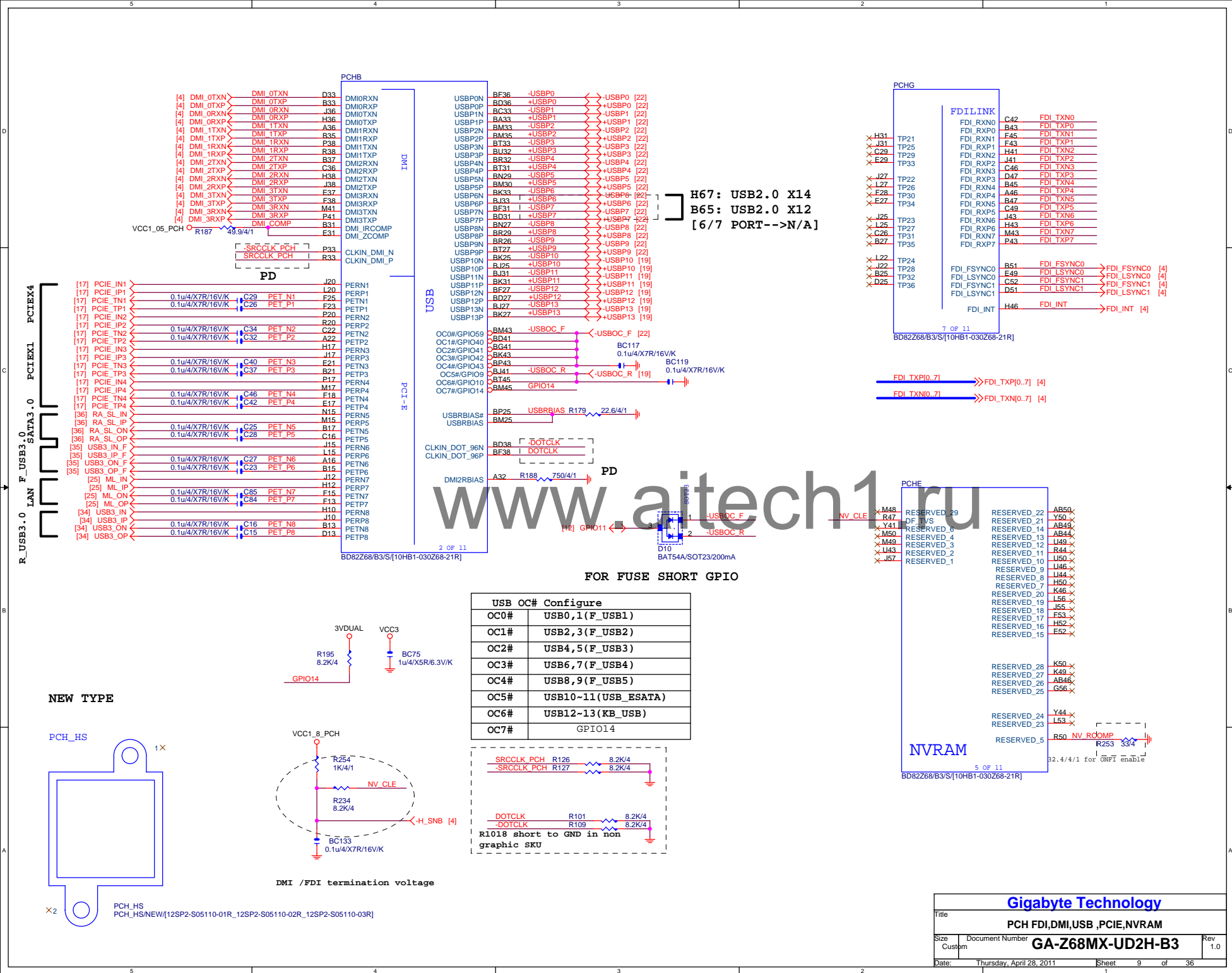


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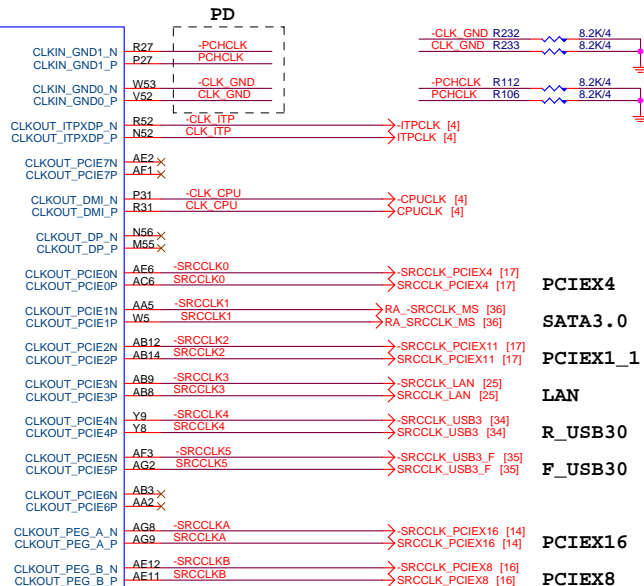
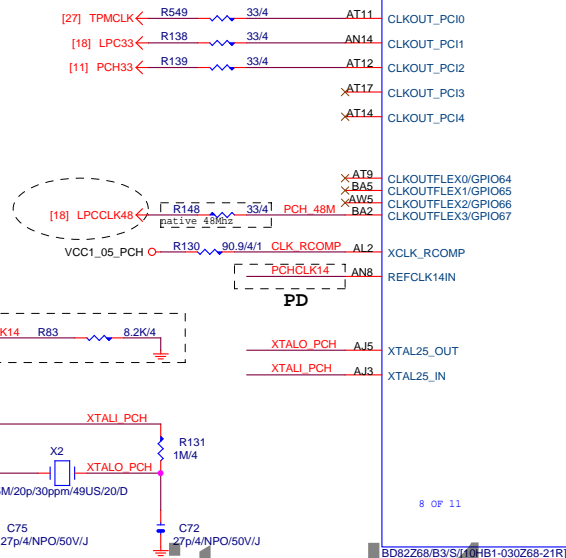
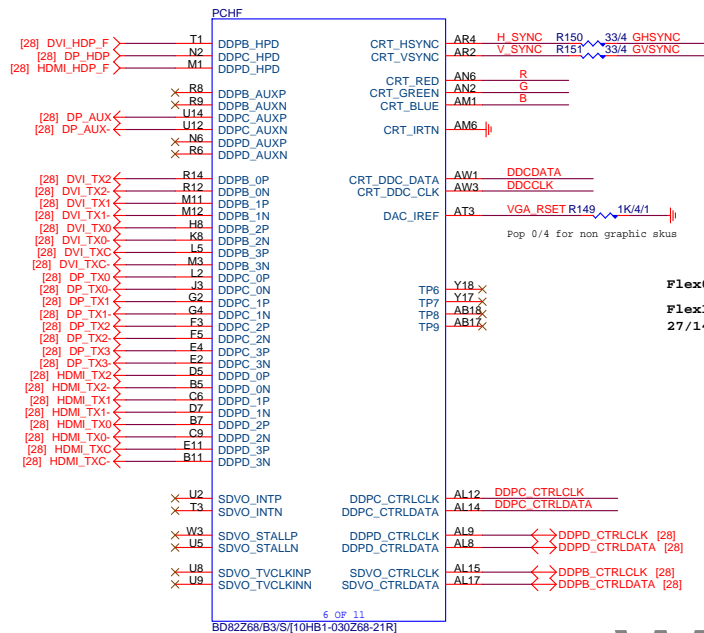
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CPU LGA1156-B			
Size			
Custom			
Document Number			
GA-Z68MX-UD2H-B3			
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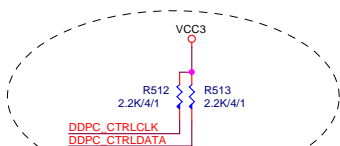




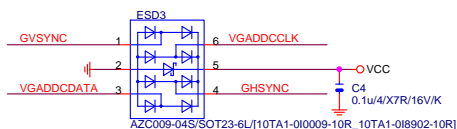
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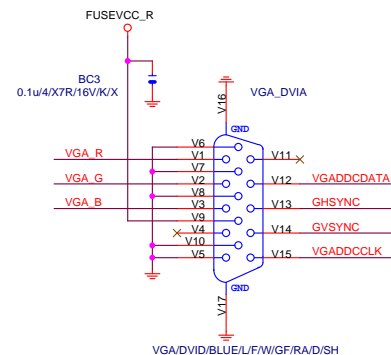
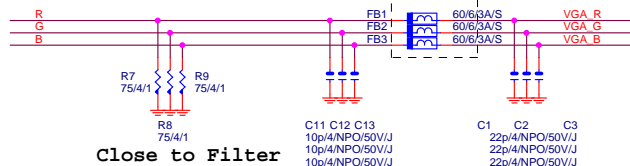
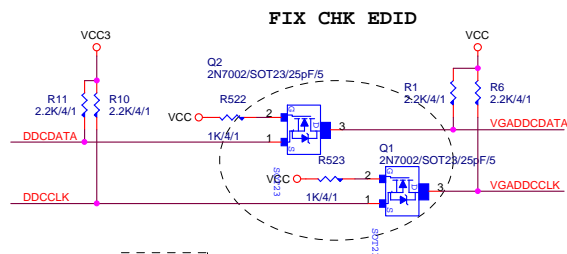
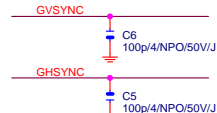
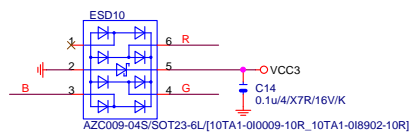
FOR OC



*DISPLAY PORT 要上件



SSOP6_ESD



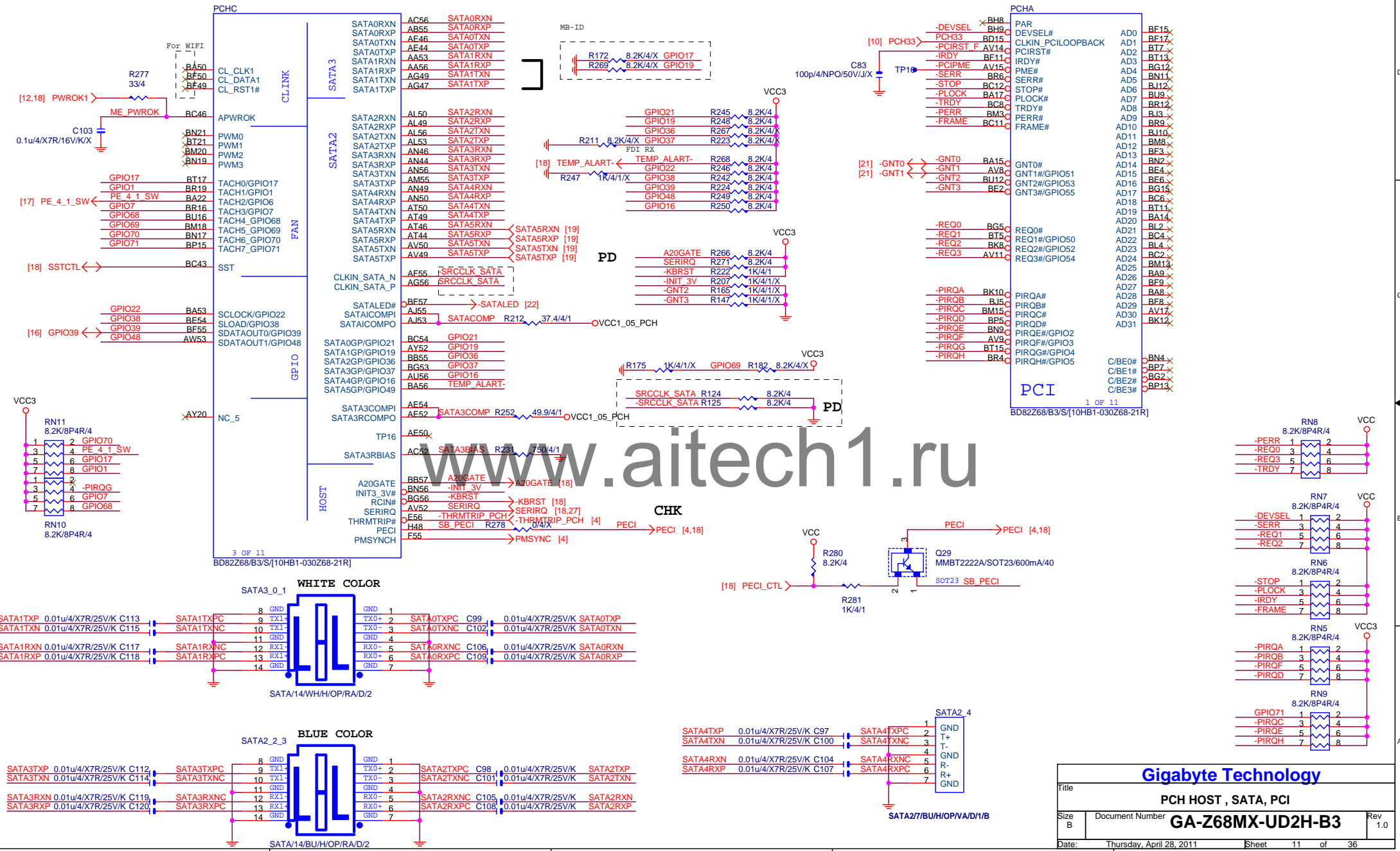
Gigabyte Technology

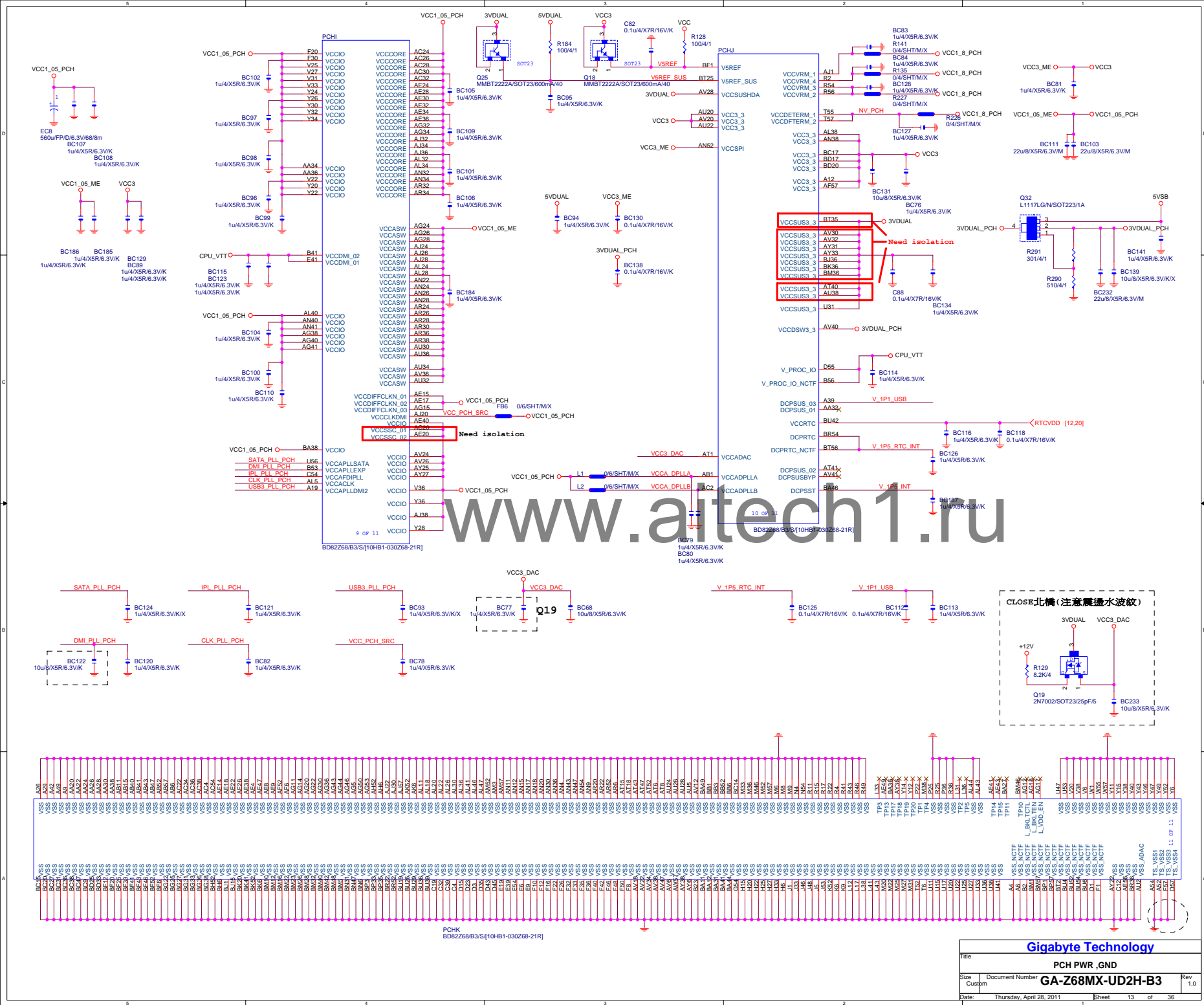
PCH DISPLAY, CLK BUFFER

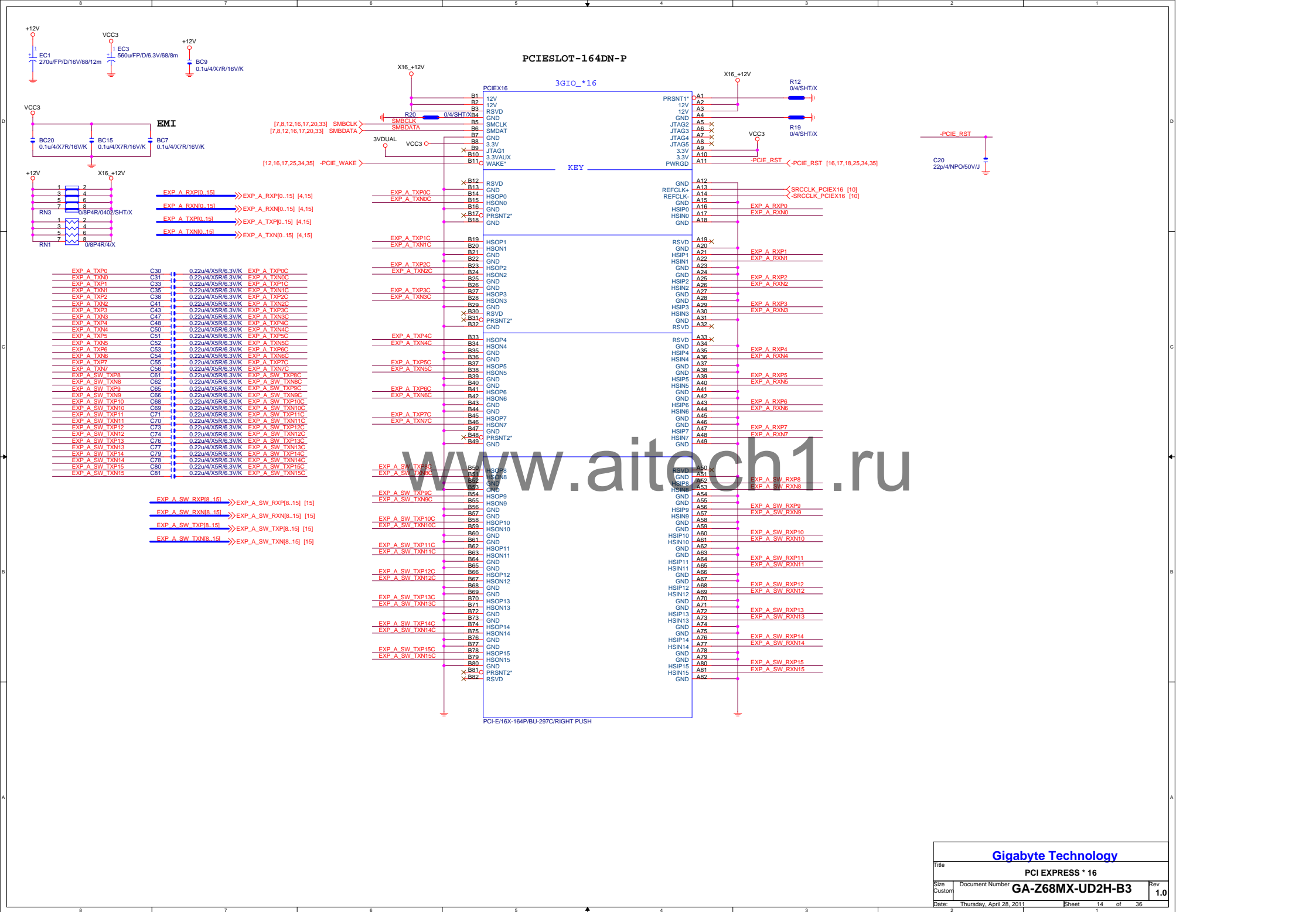
GA-Z68MX-UD2H-B3

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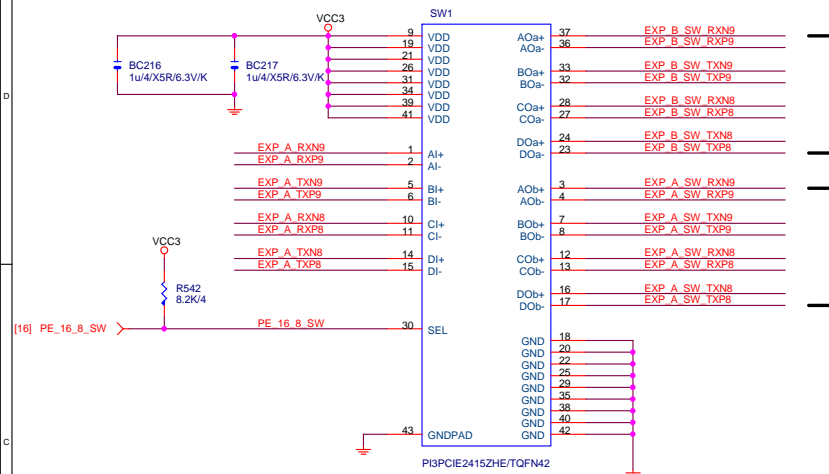
B65 SATA3.0 ONLY PORT1







Function	SEL
xI--> xOa	L
xI--> xOb	H



CPU TO SW

EXP A RXN0..15] >>> EXP_A_RXN0..15] [4,14]

EXP A TXN0..15] >>> EXP_A_TXN0..15] [4,14]

EXP A RXN12..15] >>> EXP_A_RXN12..15] [14]

EXP A TXN12..15] >>> EXP_A_TXN12..15] [14]

SW TO PCI-E X16

EXP A SW RXN8..15] >>> EXP_A_SW_RXN8..15] [14]

EXP A SW TXP8..15] >>> EXP_A_SW_TXP8..15] [14]

EXP A SW RXN12..15] >>> EXP_A_SW_RXN12..15] [14]

EXP A SW TXP12..15] >>> EXP_A_SW_TXP12..15] [14]

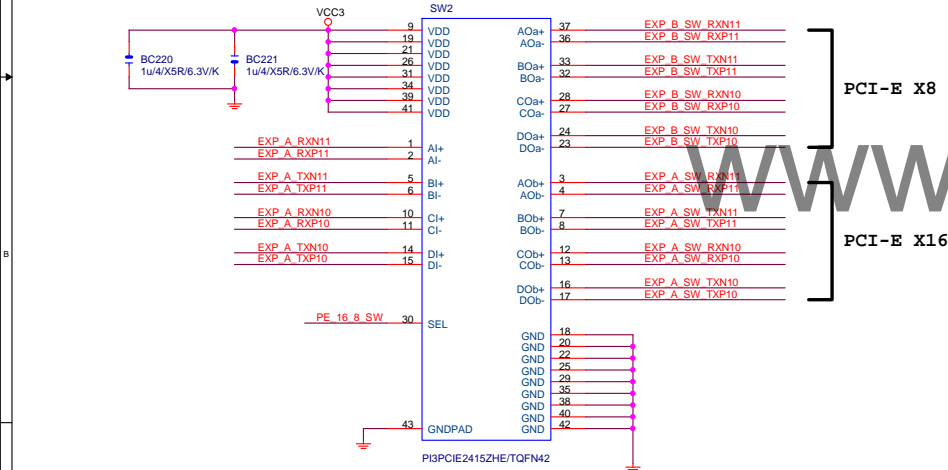
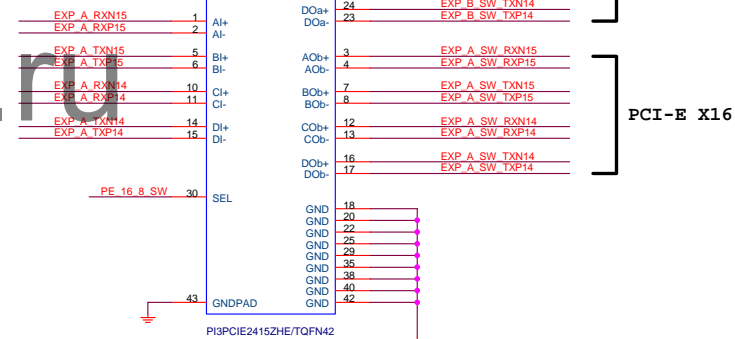
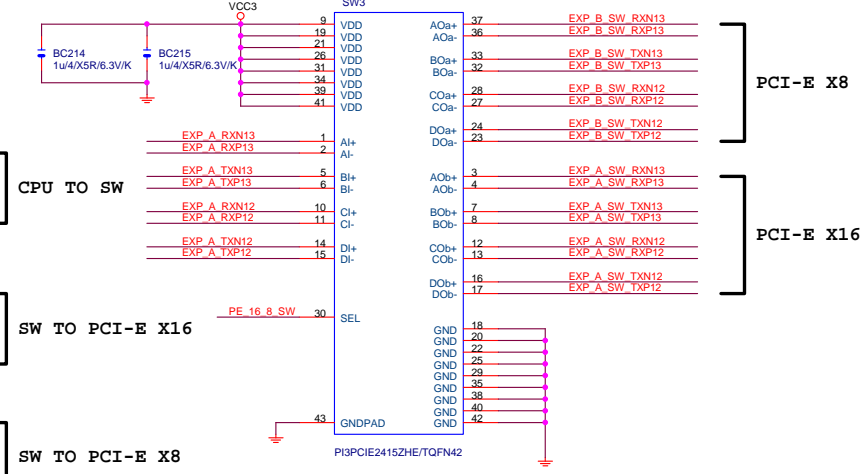
SW TO PCI-E X8

EXP B SW RXN8..15] >>> EXP_B_SW_RXN8..15] [16]

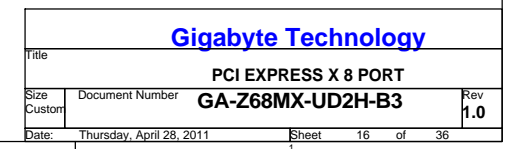
EXP B SW TXN8..15] >>> EXP_B_SW_TXN8..15] [16]

EXP B SW RXN12..15] >>> EXP_B_SW_RXN12..15] [16]

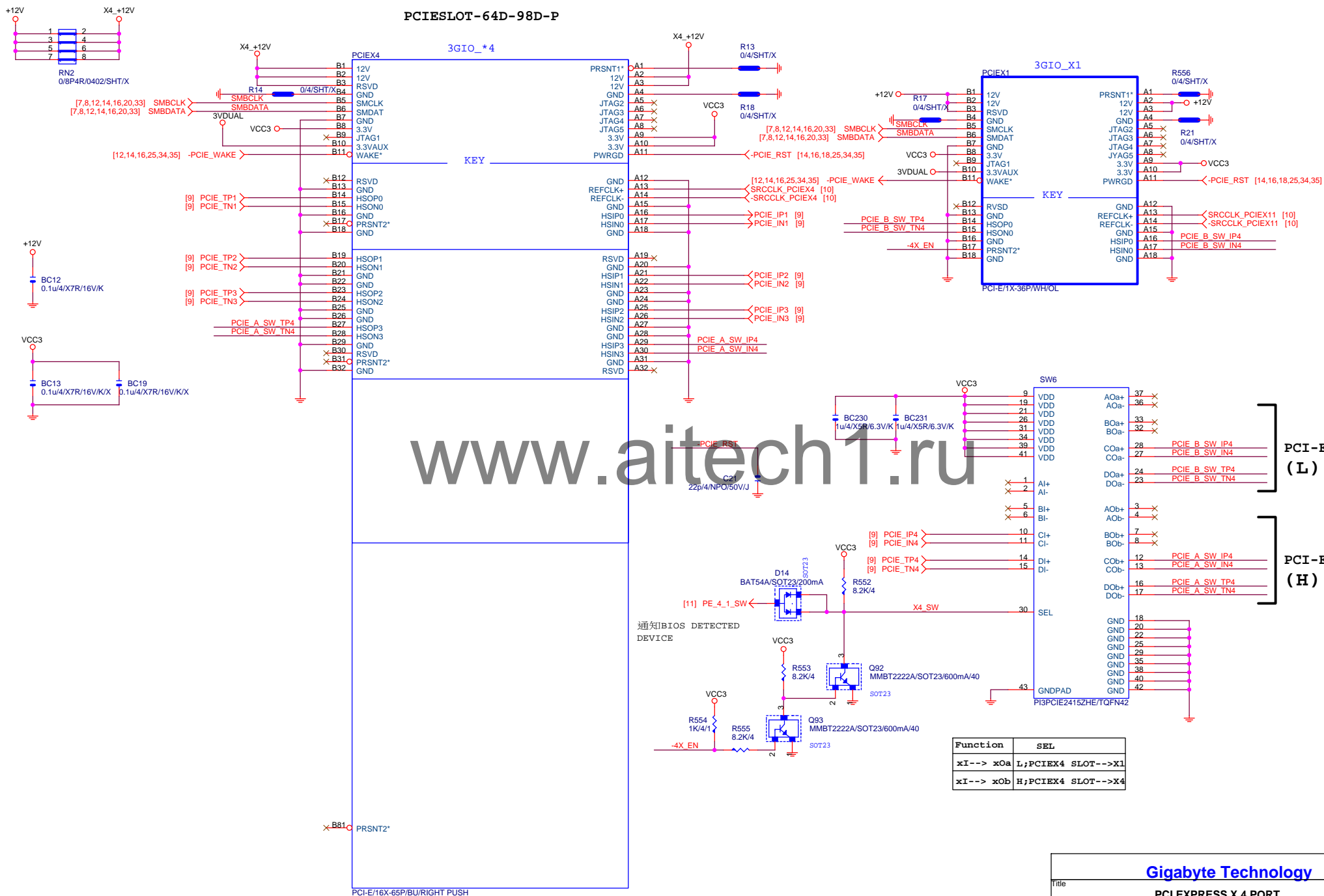
EXP B SW TXN12..15] >>> EXP_B_SW_TXN12..15] [16]



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Title: PCI EXPRESS X16 SWITCH			
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PCIESLOT-64D-98D-P



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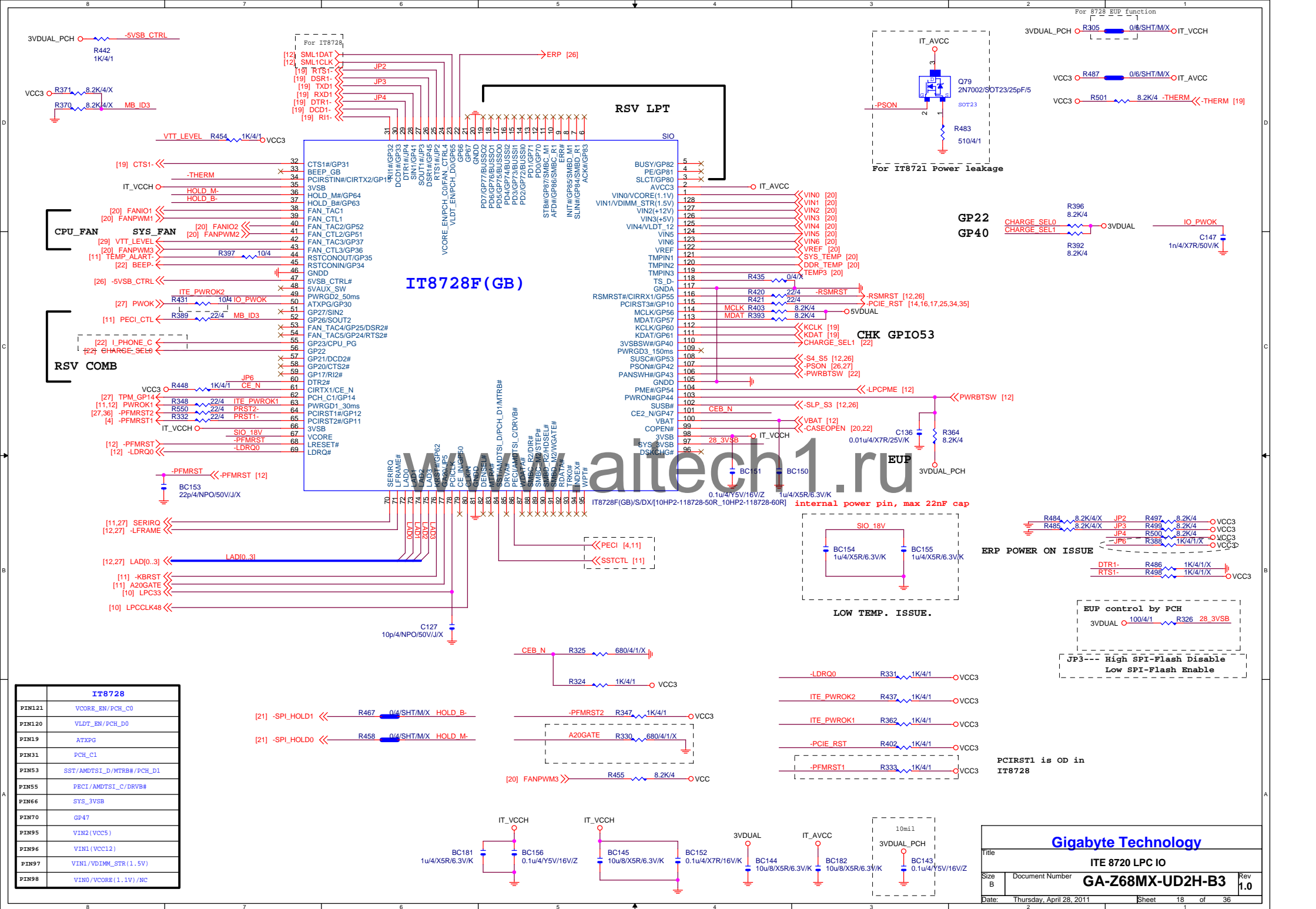
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PCI EXPRESS X 4 PORT

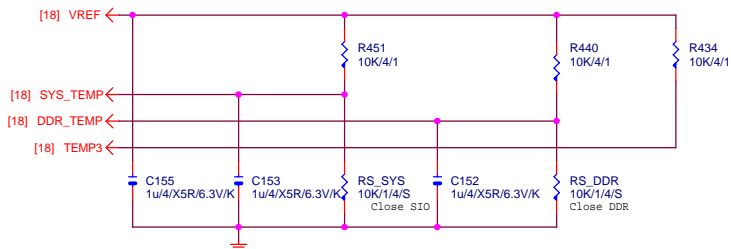
Size Custom Document Number **GA-Z68MX-UD2H-B3**

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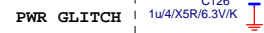
TEMP H/W MONITOR



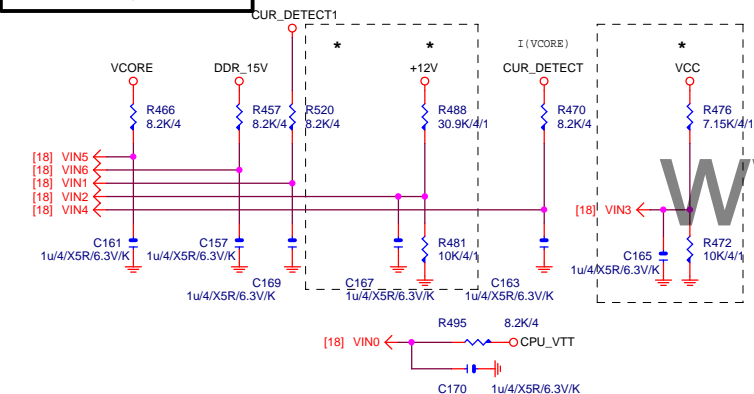
CASE OPEN



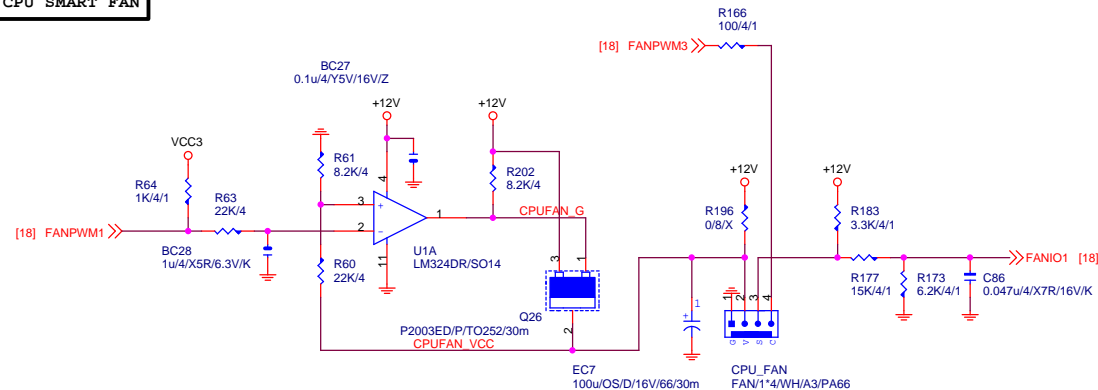
Case Open Circuits



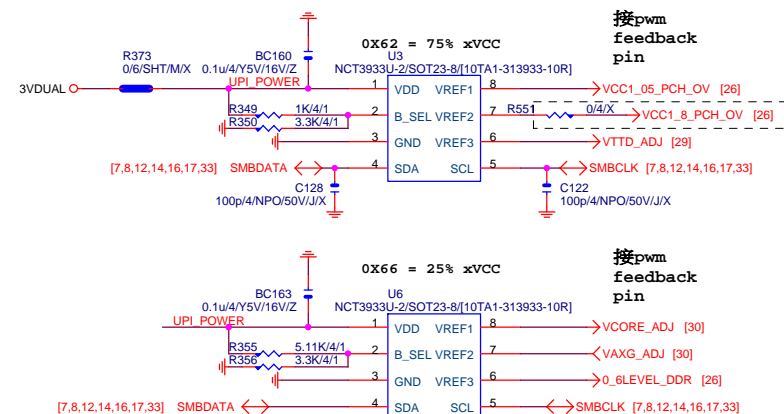
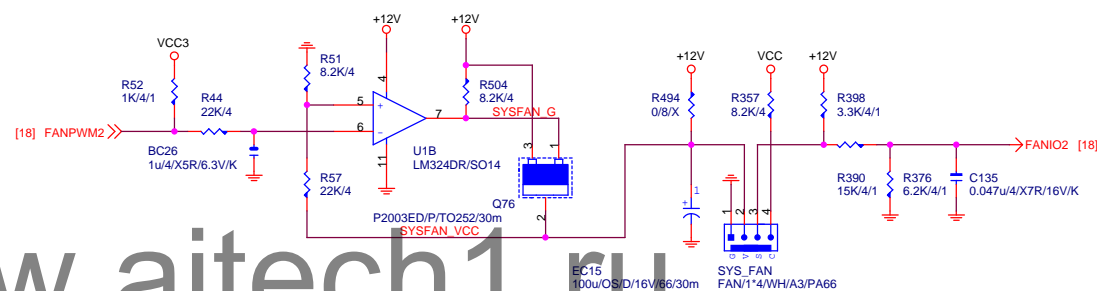
VOLTAGE-- H/W MONITOR



CPU SMART FAN



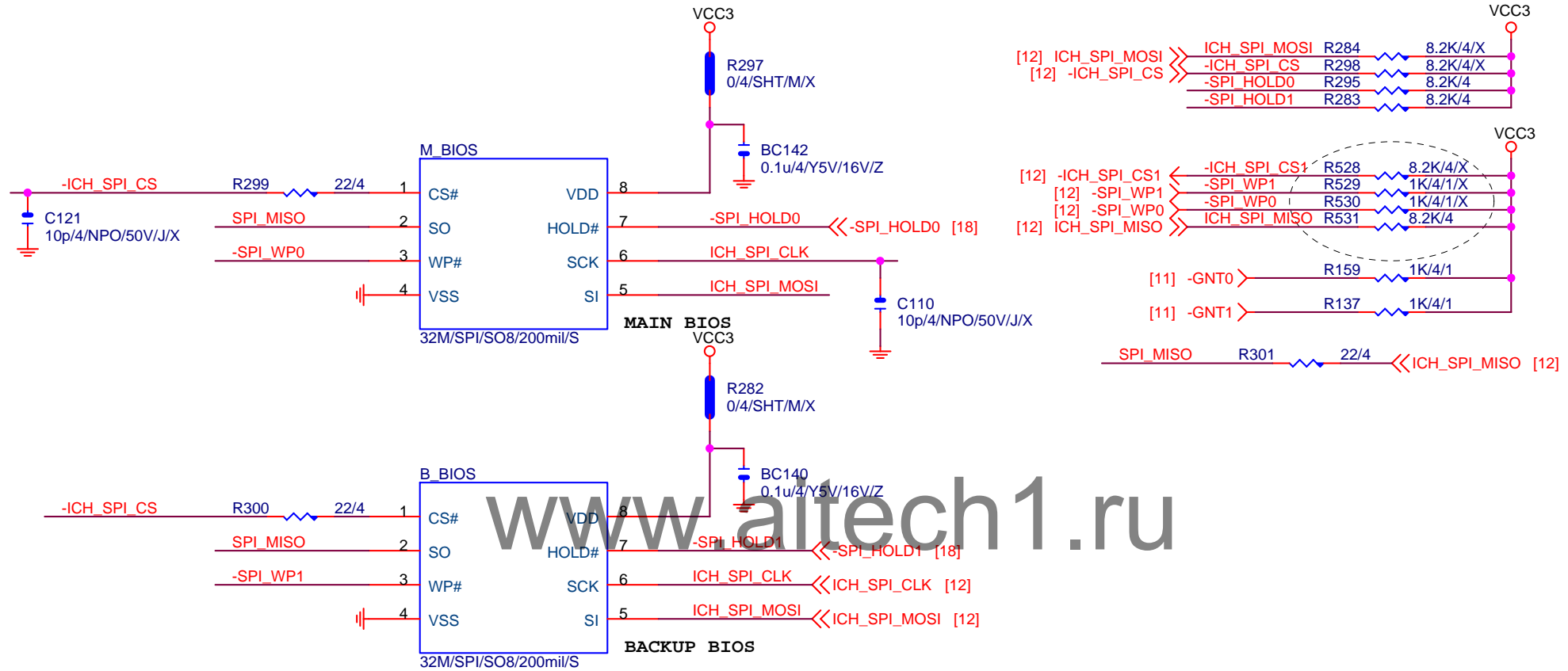
SYS SMART FAN



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Title		
HWM,FAN CTRL,OV		
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DUAL BIOS



BOOT DEVICE	GNT1	GNT0
LPC	0	0
PCI	0	1
SPI	1	1

1 means floating
0 means PD 1K

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DUAL BIOS

Title

Size
A

Document Number

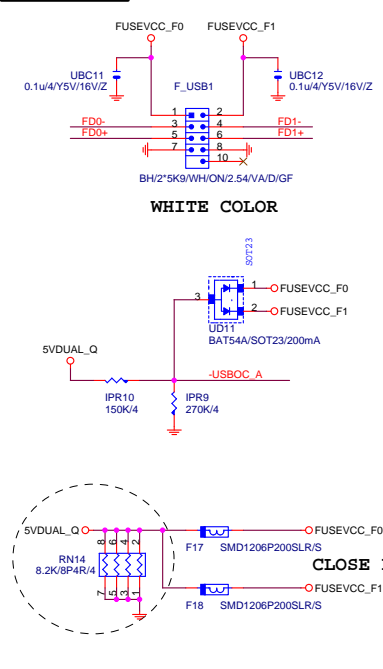
GA-Z68MX-UD2H-B3

Rev
1.0

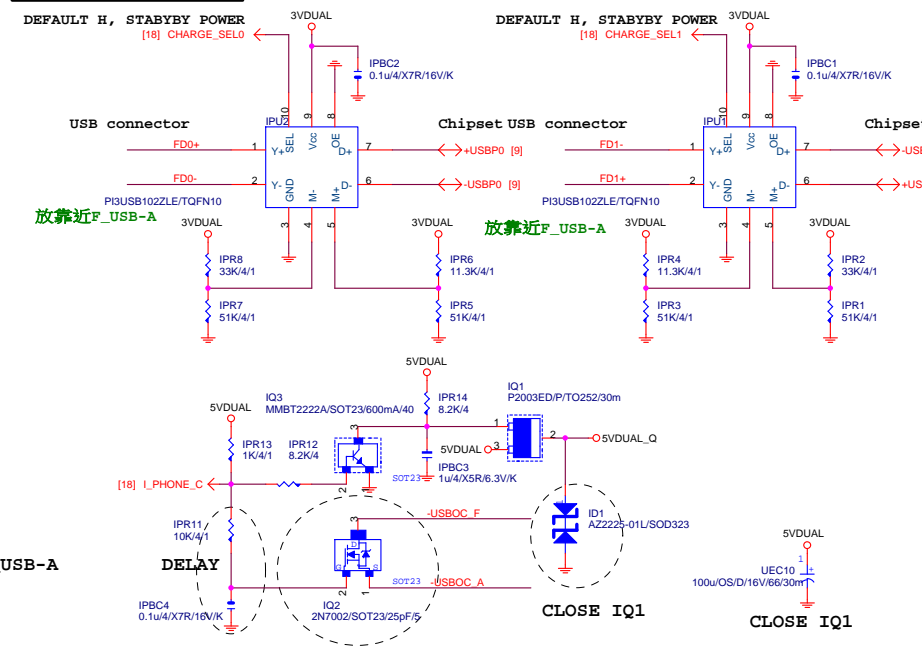
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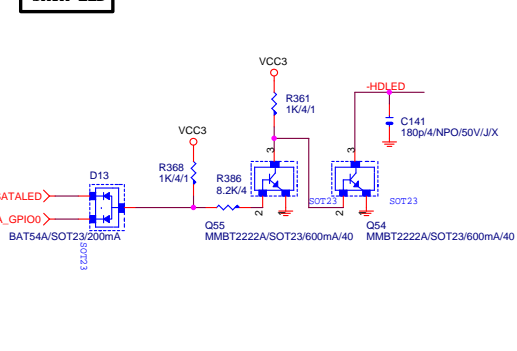
FRONT USB1



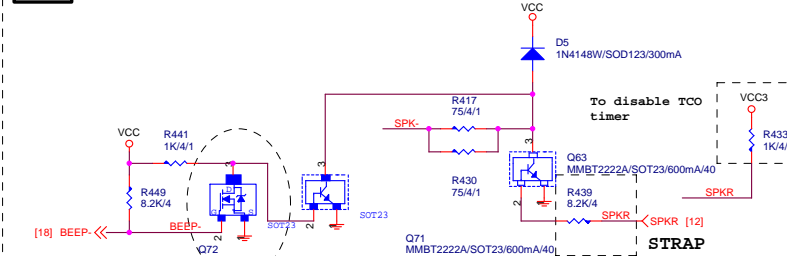
i_phone charger circuit



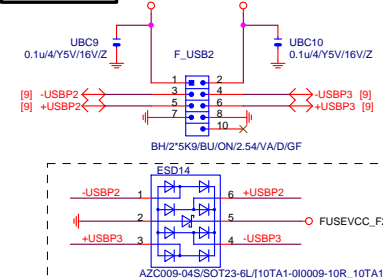
SATA LED



SPKR

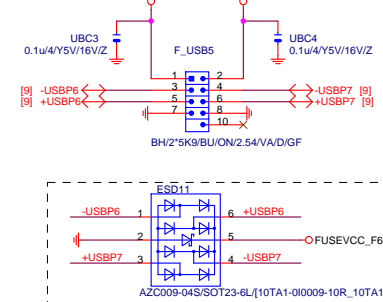


FRONT USB2



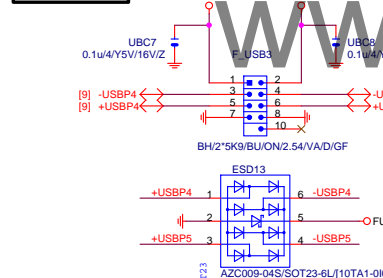
Close to connector

FRONT USB5



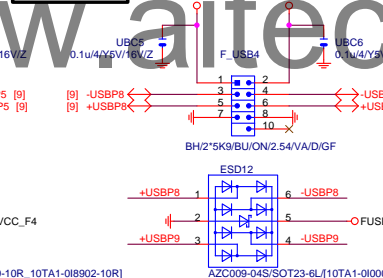
Close to connector

FRONT USB3



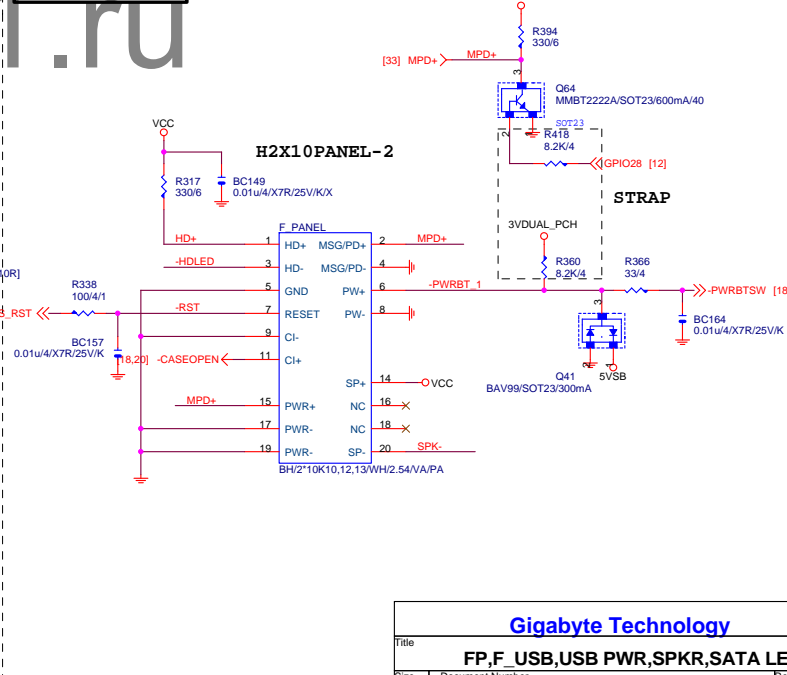
Close to connector

FRONT USB4



Close to connector

INTEL FRONT PANEL



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Title	FP,F_USB,USB PWR,SPKR,SATA LED		
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[24] CEN ←

[24] LFE ←

[24] S_SURR_L ←

[24] S_SURR_R ←

CR59 8.2K/4/X



Can Support Amp Out

HDMI SPDIF

CR52
10/4

[23] SPDIFO2_HDMI

SPDIFO_HDMI

For HDMI SPDIF

CBC31
100pF/4/NPO/50V/J

PIN

SPDIF_O
PH/1'2/BK/2.54/VA/D

For HDMI SPDIF

G3 G1

FUSEVCC_R

S1 S2 S3

[23] SPDIF

G4 G2

DP_HDMI_SPDIFC

DP+HDMI+SPDIF/20P+19P+3P/BK/RA :: Location_DP_HDMI_SPDIF

The diagram shows a 6-pin connector labeled "AZALIA JACK". The pins are arranged in a 2x3 grid. The top row contains an orange pin, a cyan pin, and a black pin. The bottom row contains a black pin, a green pin, and a pink pin. Below the connector, a detailed wiring diagram shows the connections for each pin. The pins are labeled as follows:

- Pin 1 (Orange):** LINE1_JD (Left channel line-in)
- Pin 2 (Cyan):** AJ_A5 (Left channel ground)
- Pin 3 (Black):** FRONT_JD (Front channel line-in)
- Pin 4 (Black):** AJ_B5 (Front channel ground)
- Pin 5 (Green):** MIC1_JD (Microphone line-in)
- Pin 6 (Pink):** AJ_C5 (Microphone ground)

The wiring diagram also shows the connections for the microphone and the line-in/out signals. The microphone is connected to the MIC1_JD pin (green) and the AJ_C5 pin (pink). The line-in/out signals are connected to the LINE1_JD pin (orange) and the FRONT_JD pin (black). The ground connections are shown as blue lines connecting to the AJ_A5, AJ_B5, and AJ_C5 pins.

LINE-OUT

[23] LINE_O_R

CEC6 100uF/OS/D/16V/66/30m

CR33 62/4

[23] LINE_O_L

CEC2 100uF/OS/D/16V/66/30m

CR11 62/4

CR10 10K/4/1

CR34 10K/4/1

AJ_B5

AJ_B2

CBC12 180pF/4/NPO/50V/J

CBC18 180pF/4/NPO/50V/J

Only reserved for AL888

LINE-IN

[23] LINE_IN_R

CR17 62/4

[23] LINE_IN_L

CR18 62/4

AJ_A5

AJ_A2

CBC13 180pF/4/NPO/50V/J

CBC10 180pF/4/NPO/50V/J

Verify MIC in LINE-in

For 889A/888

BAT54A/SOT23/200mA

Verify MIC function in LINE-in

For 889A/888

BAT54A/SOT23/200mA

CR17 62/4

CR18 62/4

CR3 8.2K/4

CR4 8.2K/4

CBC13 180pF/NPO/50V/J

CBC10 180pF/NPO/50V/J

AJ_A5

AJ_A2

CO1

[23] LINE_IN_R

[23] LINE_IN_L

[23] VOCR

[23] MIC1_R ← CR13 62/4

[23] MIC1_L ← CR14 62/4

[23] MIC1_VREFO_L

[23] MIC1_VREFO_R

180pF/4NPO/50V/J

CBC3

CBC2

AJ_C5

AJ_C2

[illegible]

SURR BACK

EMI

CEC1 100uF/OS/D/16V/66/30m

CEC3 100uF/OS/D/16V/66/30m

[23]_S_SURR_R

[23]_S_SURR_L

CR15 62/4

CR16 62/4

CR1 10K/4/1

B_J_A5

B_J_A2

CBC1 180pF/4/NPO/50V/J

CBC21 180pF/4/NPO/50V/J

AZALIA FRONT PANEL

F_AUDIO_H

Digital Area

Gigabyte Technology

AUDIO JACK

GA-Z68MX-UD2H-B3

Rev 1.0

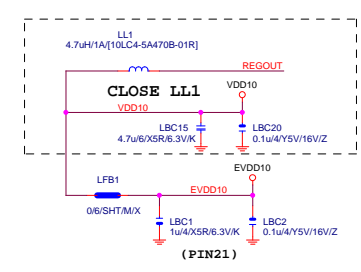
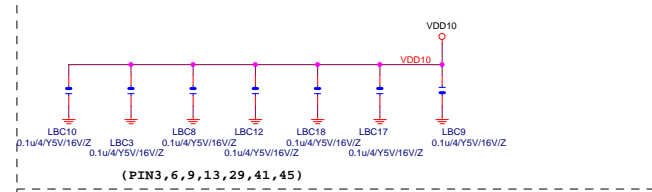
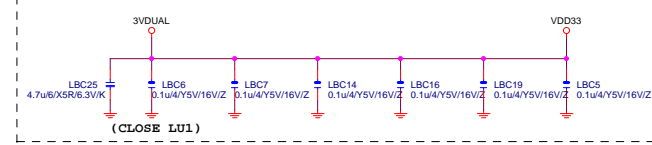
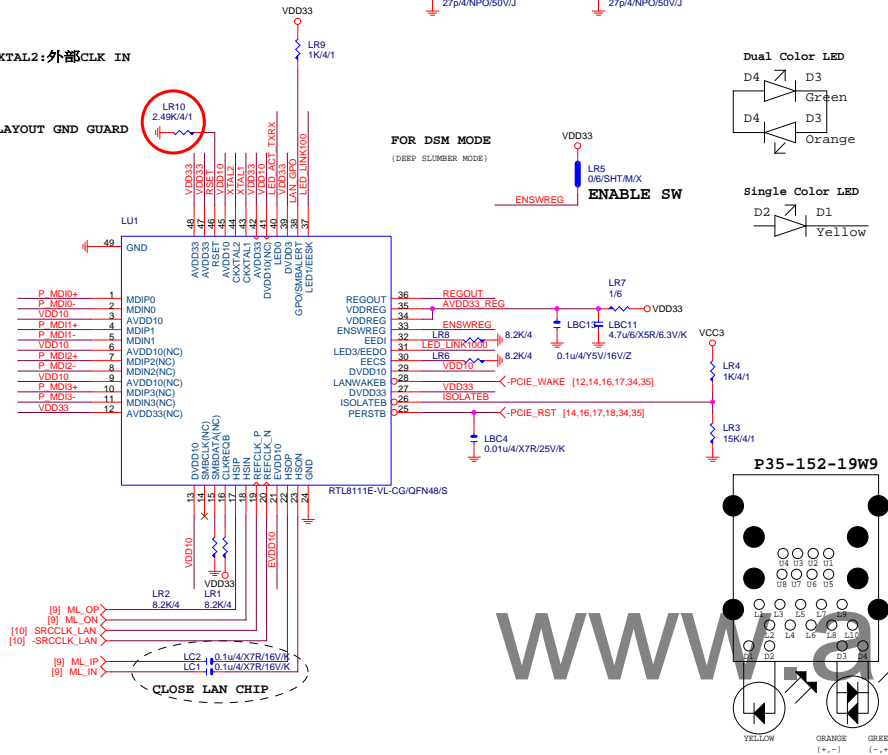
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PCIE-1G LAN

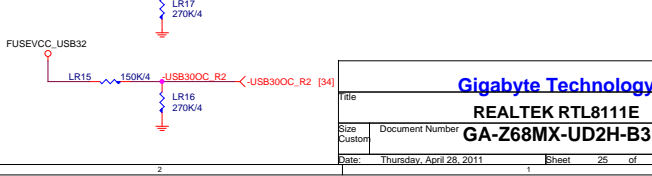
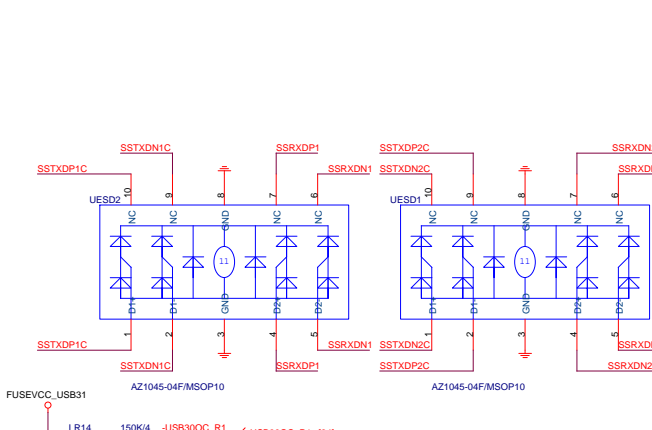
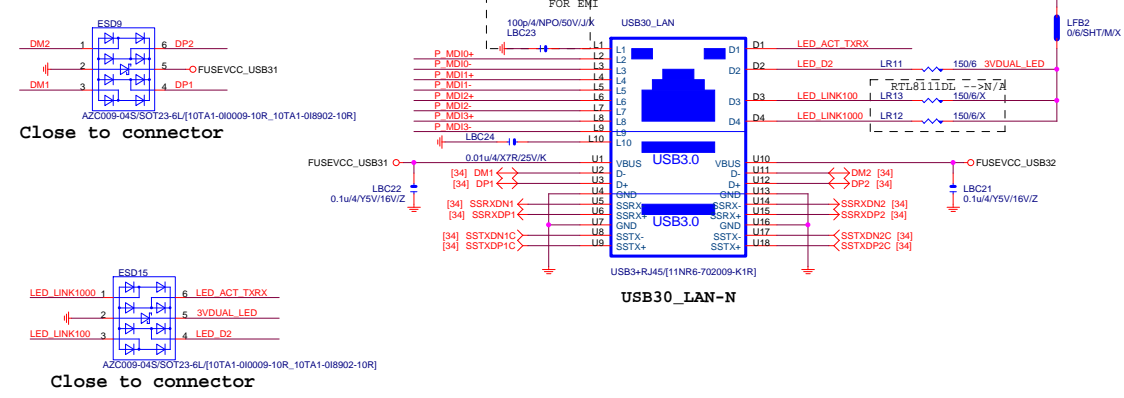
XTAL2:外部CLK IN

RSET需LAYOUT GND GUARD



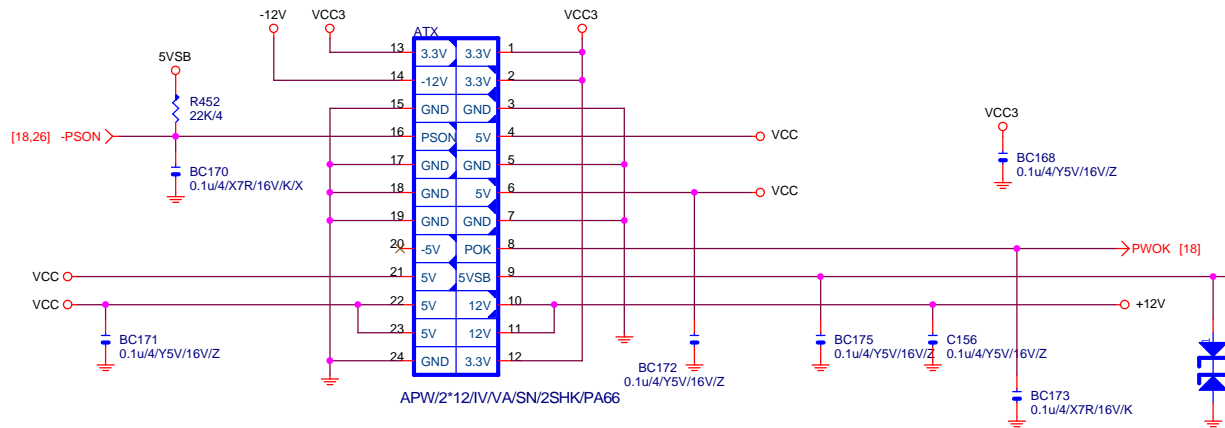
USB_LAN CONNECTOR

90欧姆: [20/4/8/4/20]

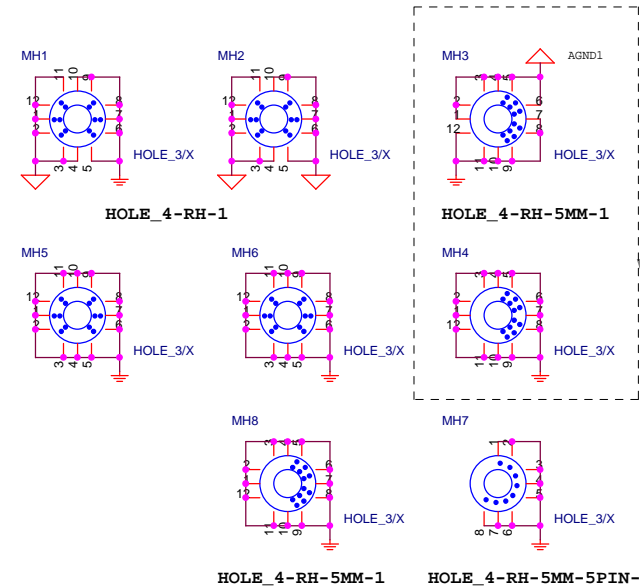
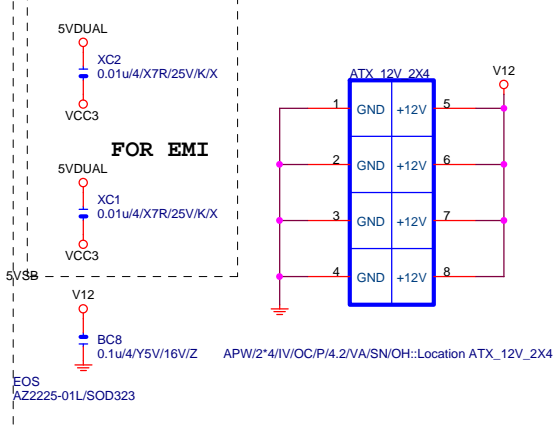


Gigabyte Technology		
REALTEK RTL8111E		
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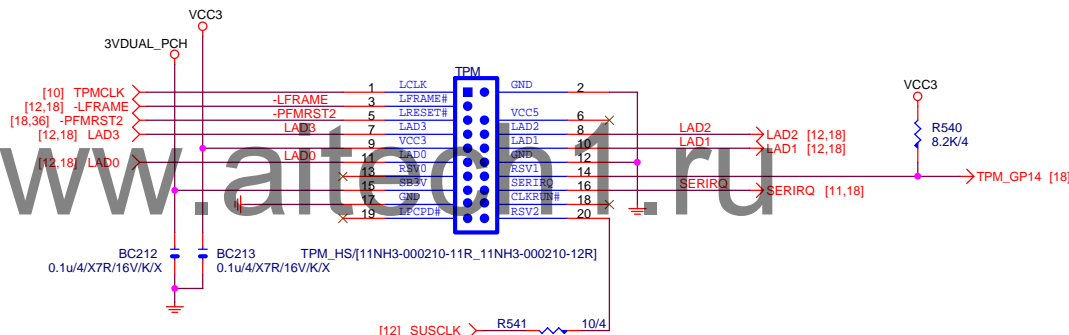
ATXX24 POWER CONNECTOR



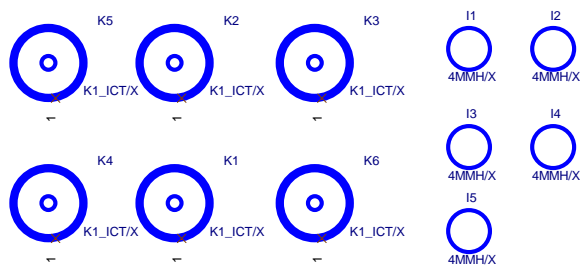
ATXX4 POWER CONNECTOR



TPM



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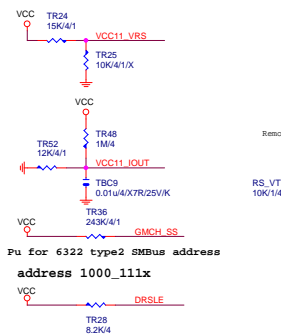


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Title	ATX CONNECTOR		
Size	Document Number	GA-Z68MX-UD2H-B3	Rev 1.0
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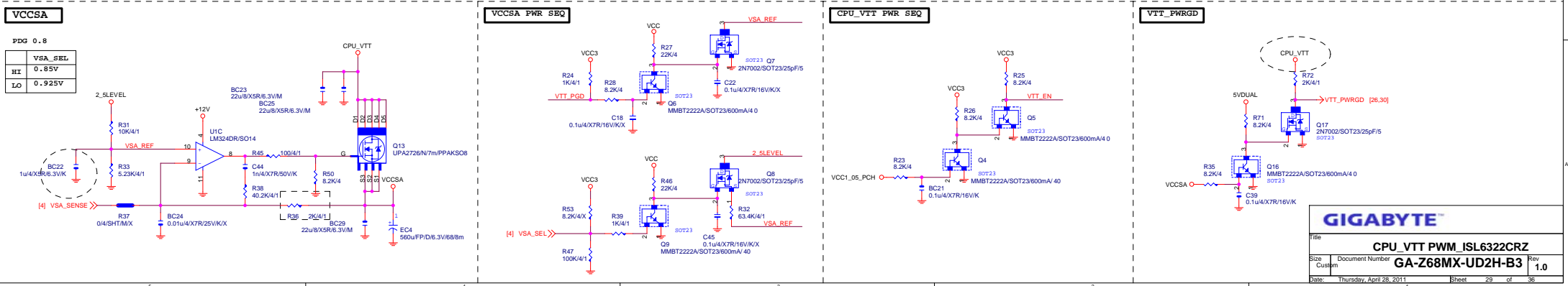
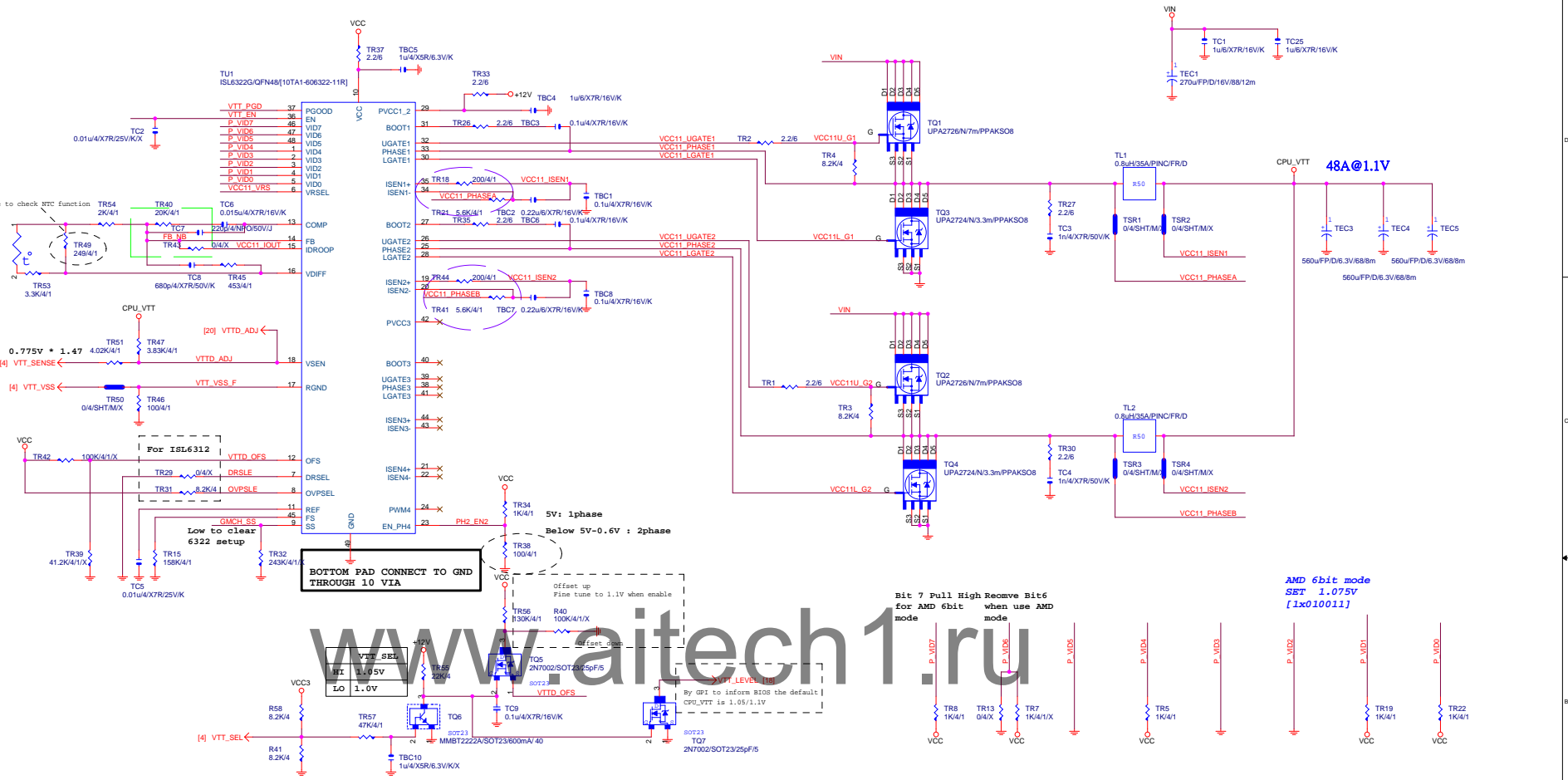
CPU_VTT

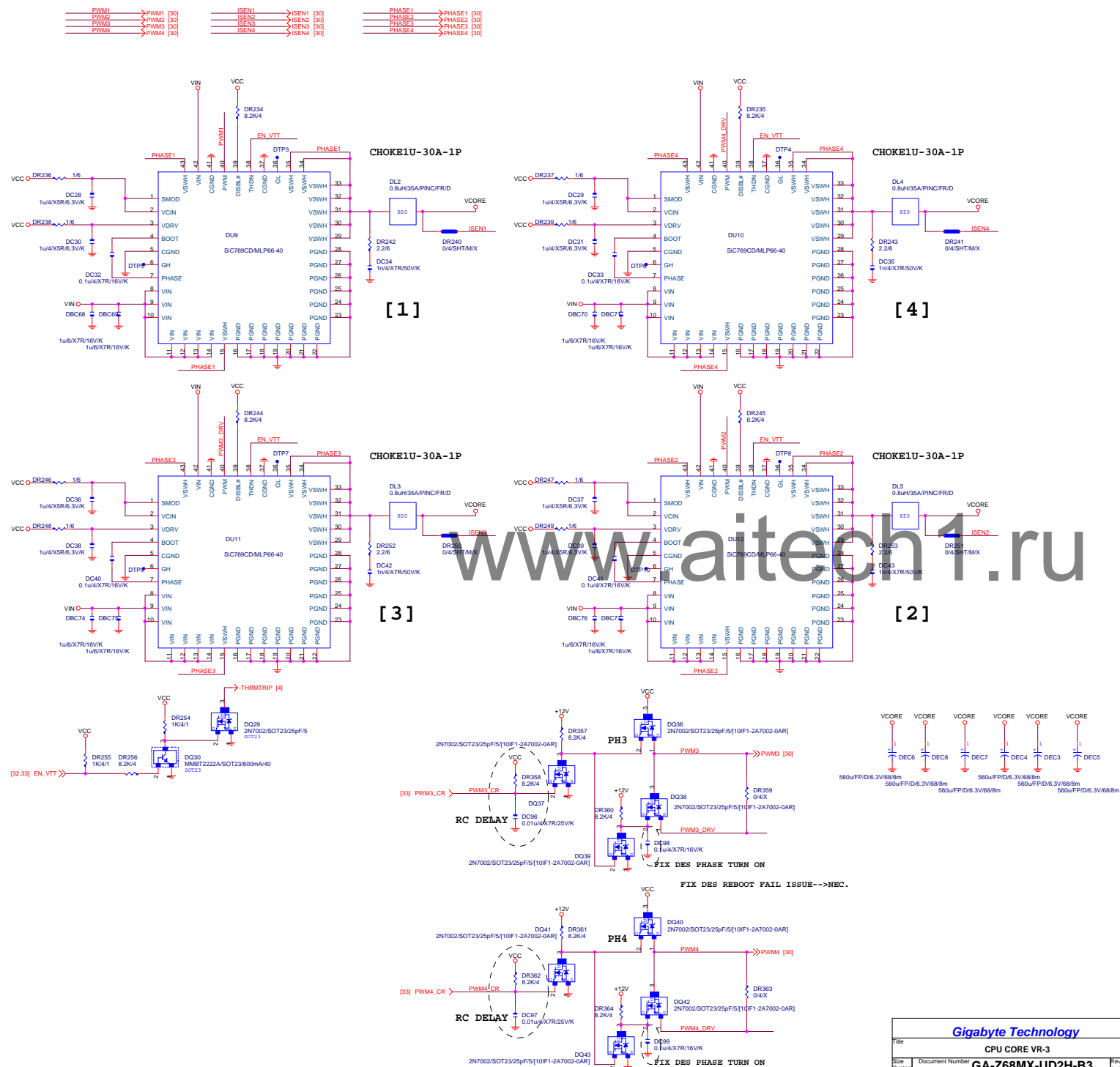
5V : AMD mode
0.6V~3V : VRD11 mode
0V : VRD10 mode



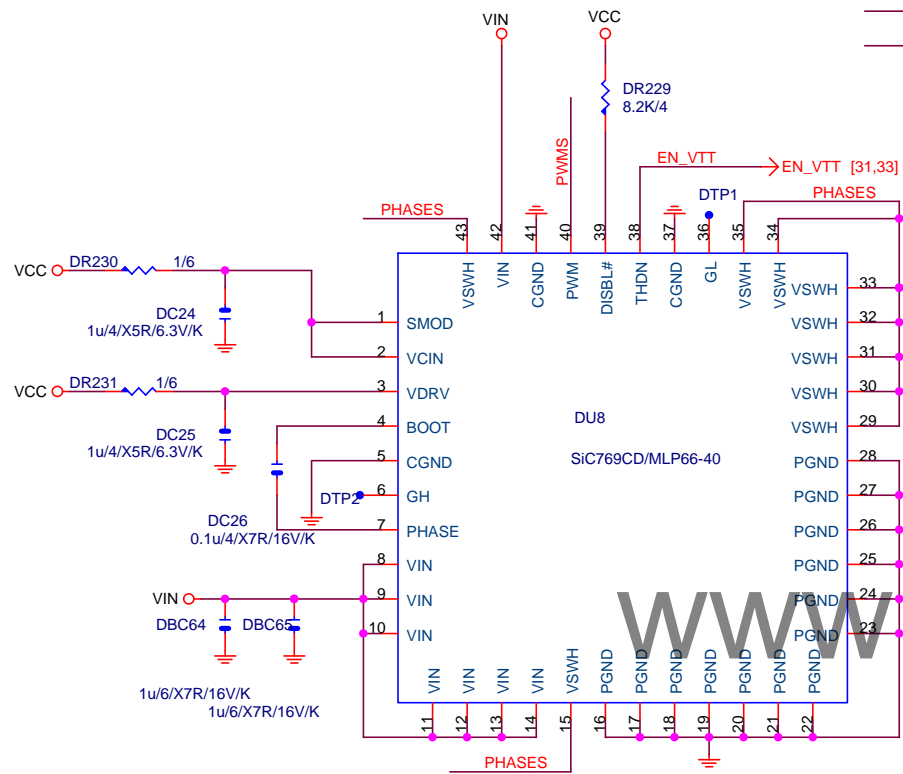
Pu for 6322 type2 SMBus address
address 1000_111x
VCC11_IIN

OCP點做在146A
Isens+ R270阻值設在590ohm
Iocp=(IsensxRisenxPhase)/DCR
=[(120uAX590X2)/0.97m=146A
L/DCR=RxC
L=1uH DCR=0.97 mohm ,
1uH/0.97mohm=4.7kX0.22uF
Risens R260 阻值=4.7k ohm, Cisen
BC75=0.22u
Rt=10^{0.61-[1.035xlog(FS)]}
Rt=R301=158 kohm , FS=170KHz
OVP=VDAC+225mV





VAXG

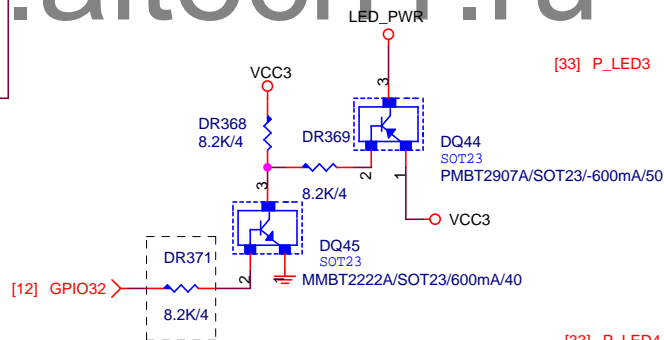


CHOK1U-30A-1P

DL6
0.8uH/35A/PINC/FR/D

DR233
2.2/6
DC27
1n4/X7R/50V/K

LED POWER



PHASE LED

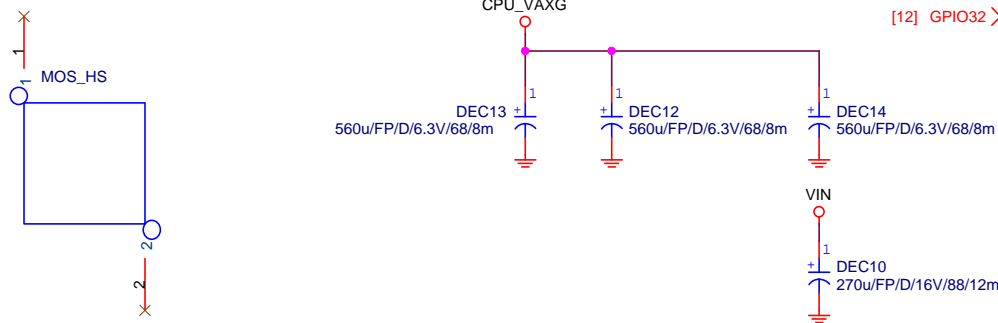
LED_PWR
DR365
220/6
STAGE1
DD1
LED/G/6/S

LED_PWR
DR366
220/6
STAGE2
DD2
LED/G/6/S

LED_PWR
DR367
220/6
STAGE3
DD3
LED/Y/6/S

LED_PWR
DR370
220/6
STAGE4
DD4
LED/R/6/S

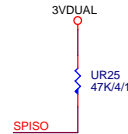
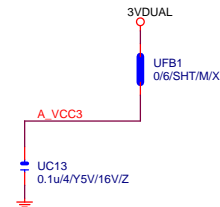
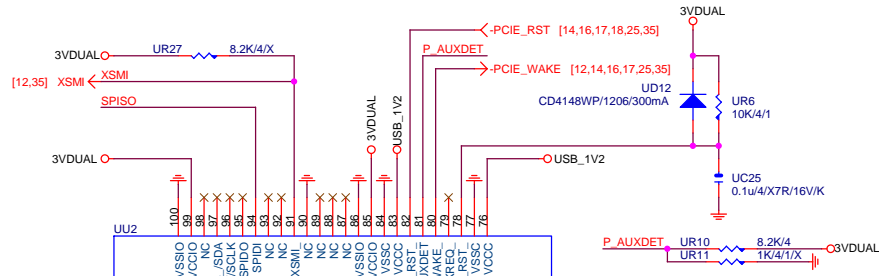
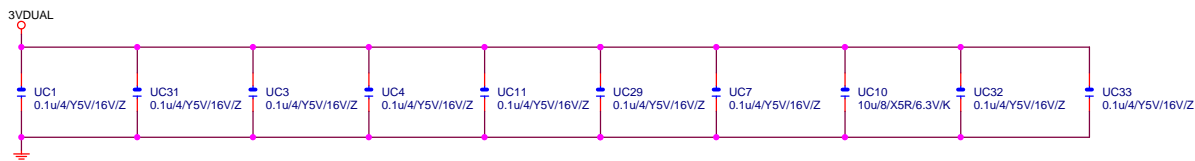
MOS HEATSINK



MOS HS/[12SP2-S06928-01R_12SP2-S06928-02R_12SP2-S06928-03R]

Gigabyte Technology

Title			CPU CORE VR-2
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Custom			Rev 1.0
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SPIIM: Low=>SPI Rom.

UR9 8.2K/4

USB_1V2

UR9 8.2K/4

UR9 8.2K/4

UR9 8.2K/4

UR9 8.2K/4

UR9 8.2K/4

UR9 8.2K/4

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UR9 8.2K/4

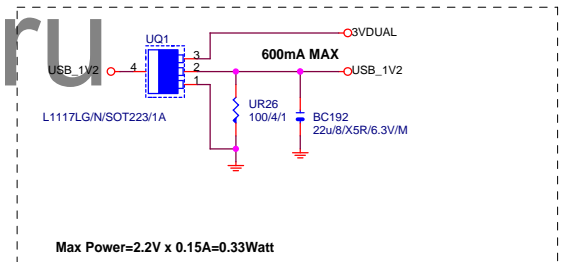
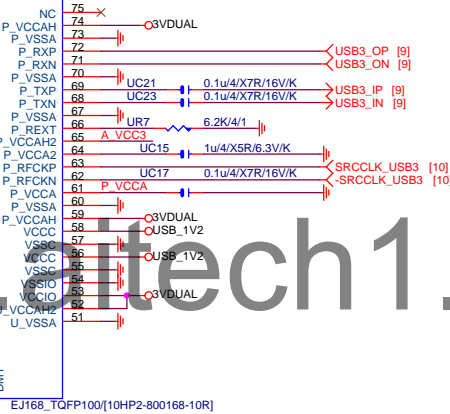
UR9 8.2K/4

EJ168

3VUDAL=550mA max

USB1V2=150mA max

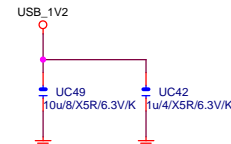
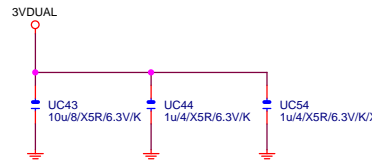
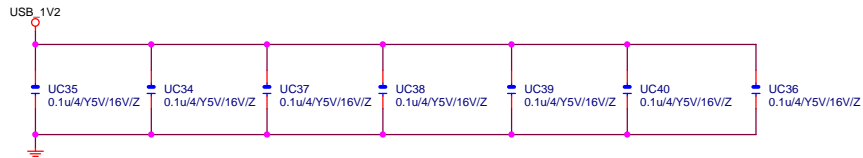
www.gigabyte1.ru



Max Power=2.2V x 0.15A=0.33Watt

AZ1117H-1.2TR/SOT223/1A-->UR17:0/4,UR16:N/A [1.2V]

L1117LG/N/SOT223/1A-->UR17:0/4,UR16:100/4/1 [1.25V]



GIGABYTE

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F_USB3.0 EJ168			
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